3.6 A 0.5V 74dB SNDR 25kHz CT ΔΣ Modulator with Return-to-Open DAC

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The continuous reduction of minimum feature sizes in modern CMOS technologies into the nano-scale requires a proportional reduction of the supply voltage to well below 1V to maintain reliability. At the same time, the threshold voltage of the devices is not scaled in the same proportion to limit leakage currents for digital circuits. The combination of low supply voltages and high device thresholds poses very challenging constraints on the analog circuit design. In this paper, a 0.5V CT 3rd-order ΔΣ modulator is presented that is implemented in CMOS and does not use any special low-voltage devices and no internal voltage boosting. As such, the design is compatible with the supply voltage constraints of future nano-scale CMOS processes.

Figure 3.6.1 shows the fully differential implementation of the 3rd-order modulator with active-RC integrators. The ratios between the resistors set the CT modulator coefficients which have been obtained from a discrete-time prototype with an impulse response-invariant transformation taking into account the feedback DAC waveform. The signal bandwidth is set to 50Hz to 25kHz with a sampling frequency of 3.2MHz for an OSR of 64. Input resistors R1bp, R1bn, R1ap, and R1an are scaled such that the modulator is stable with a $1V_{pp\text{-}diff}$ input. The thermal noise from these resistors limits the SNR to 81dB for a $1V_{pp\text{-}diff}$ input. System-level simulations further shows that an SNDR of 77dB can be maintained for an RC time-constant variation of ±40%, and thus frequency tuning is not required.

The fully differential implementation reduces the distortion due to asymmetries between the rising and falling edges of the DAC signal. The DAC clock φ_{DAC} is delayed by 10% of the clock period (T) from the comparator clock φ to allow the comparator output to fully settle before the DAC becomes active. To avoid distortion degradation due to ISI an RZ DAC pulse with 50% duty cycle is used. For V_{DD}=0.5V standard MOS devices with threshold voltages of $|V_{TP}| \approx V_{TN} \approx 0.5V$ at zero body-source voltage cannot be used to switch the DAC output to the input CM of $V_{DD}/2$. Switching the DAC output to GND or V_{DD} would also offer the benefits of RZ signaling but would exercise the CM response excessively.

To enable the ultra-low voltage operation a "return-to-open" (RTO) signaling scheme is developed. During the RZ intervals, the DAC output is open circuited and left floating. No current from the DAC flows into the integrating capacitors and the DAC output voltages are reset to the input CM voltage of the integrator amplifier. The RZ effect is obtained without the need for switches that are connected to $V_{DD}/2$. Figure 3.6.2 shows the RTO DAC circuit with the reference voltages V_{REFP} and V_{REFN} set to V_{DD} and GND, respectively. The body terminals of the transistors are biased at $V_{DD}/2$ to lower their $|V_T|$ and to ensure proper logic gate operation at the required clock speed. The RTO DAC consists of two clocked inverters connected in series and an internal reset switch M4. For φ low, M3 and M7 turn off and nodes 1 and 2 float. For φ high, nodes 1 and 2 are connected to V_{REFP} or to V_{REFN} depending on the comparator output, Q. The C_{gd} of M1 and M2 introduce a signal-dependent charge injection into node 1 during the RZ intervals. Switch M4 always resets the input of the second stage (M5-M7) to V_{REFP} to make the parasitic charge injection into the integrating capacitors through the C_{gd} of M5 and M6 signal-independent.

If a single RTO DAC drives all feedback resistors, the internal signals in the three integrators (Fig. 3.6.1) couple through the DAC output node when it floats. This alters the transfer function of the loop filter and significantly degrades the performance of the modulator. Splitting the RTO DAC into independent sections by implementing a separate second stage buffer M5-M7 for each feedback resistor eliminates this coupling (Fig. 3.6.1). The number of buffers is increased, but the transistor sizes for each buffer can be reduced because of the smaller load. A single phase 0 to V_{DD} square wave external clock source is used and all necessary clock phases are generated on chip with special care in keeping jitter as low as possible.

A standard latched comparator circuit that operates from a 0.5V supply becomes very slow because all transistors operate in weak inversion. The comparator in Fig. 3.6.3 uses the transistor bodies for the input signal and the transistor gates for the clock and consists of a pre-amplifier that is active for φ low and a latch stage that is active for φ high. A two-stage body-input OTA is designed based on the topology in [1] in combination with automatic biasing circuits, as in [2], that adjust the output CM voltage to $V_{DD}/2$ against PVT variations. In the first stage OTA design special care is given to reduce its 1/f noise. Measurements on a replica of this OTA give a dc gain of 46dB, a unity-gain bandwidth of 4.0MHz, and a differential input-referred noise voltage of $33nV_{rms}/\sqrt{Hz}$ and $12nV_{rms}/\sqrt{Hz}$ at 10kHz and 1MHz, respectively. In many building blocks the body terminal is used for signal input or for $|V_T|$ reduction. With a V_{DD} of 0.5V the risk of substantially forward biasing the junctions or triggering latch-up is minimal, assuming the supply over-voltage transients are kept under control [1, 2, 3].

A prototype modulator is designed in a 0.18μm triple-well CMOS technology using only standard NMOS and PMOS transistors. Figure 3.6.7 shows the die micrograph; the modulator core occupies an area of $0.6mm^2$. Six packaged ICs are tested and all performed very closely. The typical modulator performance at room temperature is summarized in Fig. 3.6.6. For the nominal V_{DD} of 0.5V a peak SNDR of 74dB is achieved in a 25kHz bandwidth for a full range differential input signal of $1V_{pp\text{-}diff}$ with a power consumption of 370μW that includes 70μW of the large measurement output buffers. The modulator output spectrum computed off-line from a captured bit stream with Blackman windowing is shown in Fig. 3.6.4. The SNDR for varying input levels is presented in Fig. 3.6.5. The modulator performance for supply voltages from V_{DD}-10% to V_{DD}+60% is close to its nominal performance. The measured performance of the modulator further remains close to, or exceeds, its nominal performance for a temperature range from 20 to 80°C.

Acknowledgments:
The authors thank Professor Y. Tsividis and Professor J.E. Franca for their support; Professor M. Steyaert for help with packaging; and, A. Jha and J. Shen for their assistance with the measurements. Hong Kong RGC (Project No.CUHK4202/03E) and Analog Devices have provided financial support for parts of this work.

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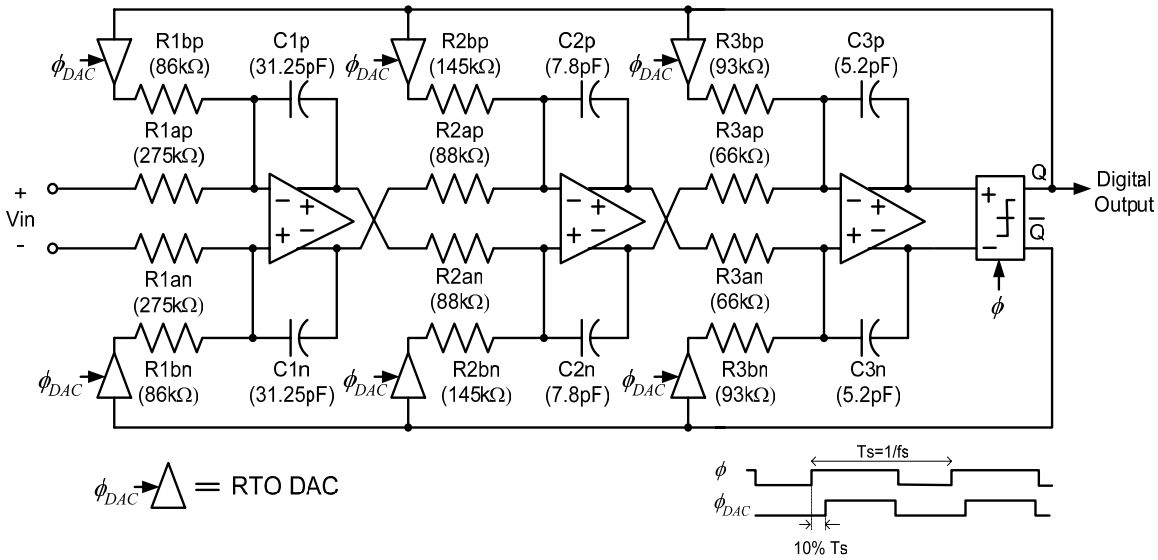

Figure 3.6.1: Architecture of the 0.5V 3rd-order CT ΔΣM.

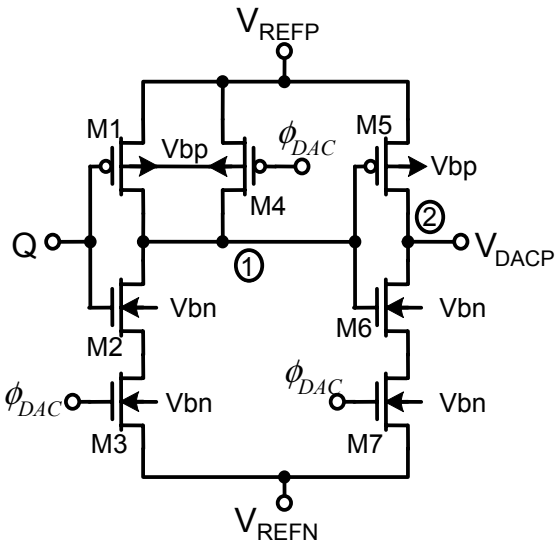

Figure 3.6.2: Return-to-open DAC circuit.

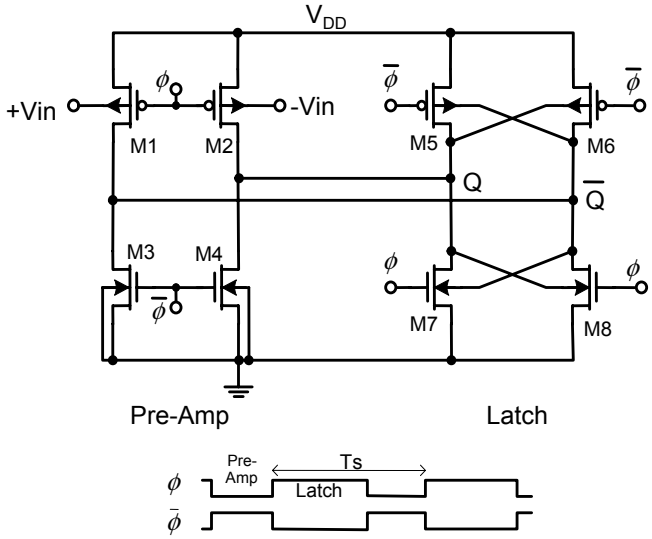

Figure 3.6.3: Body-input gate-clocked comparator.

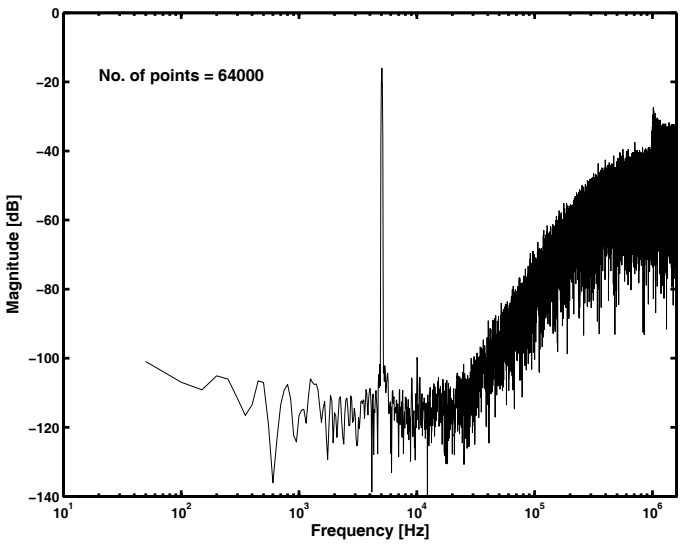

Figure 3.6.4: Measured output spectrum for a -4dBV$_{ref}$ input (V$_{ref}$= 1V$_{pp-diff}$).

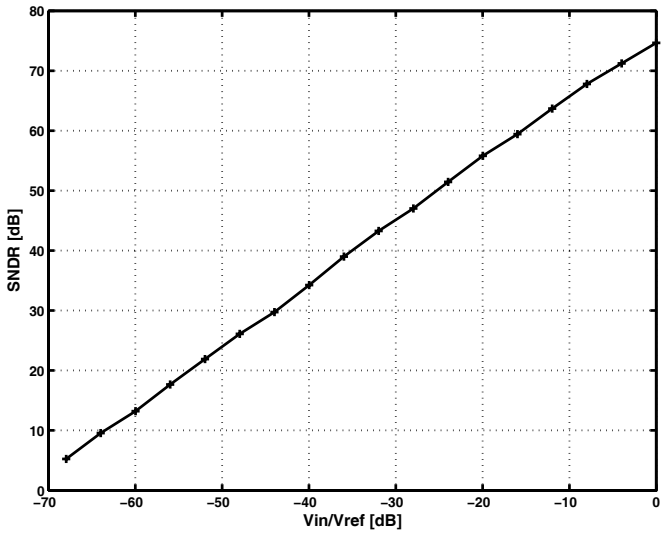

Figure 3.6.5: Measured SNDR versus V$_{in}$(V$_{ref}$= 1V$_{pp-diff}$).

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Modulator type	1b, 3rd-order, continuous-time		
Signal bandwidth	25kHz		
Sampling frequency/OSR	3.2MHz / 64		
Input range	$1V_{pp\text{-}diff}$		
Supply Voltage	0.45V	**0.5V**	0.8V
SNDR @ Vin = $1V_{pp\text{-}diff}$	71 dB	**74dB**	74dB
SNR @ Vin = $1V_{pp\text{-}diff}$	76 dB	**76dB**	74dB
Power consumption (total) ΔΣ Modulator (filter + comparator + DAC) Output buffers		**370μW** **300μW** **70μW**	
Active die area	0.6mm²		
Technology	0.18μm CMOS (standard V_T, triple-well, MIM, and HiRes Poly)		

Figure 3.6.6: Performance summary.

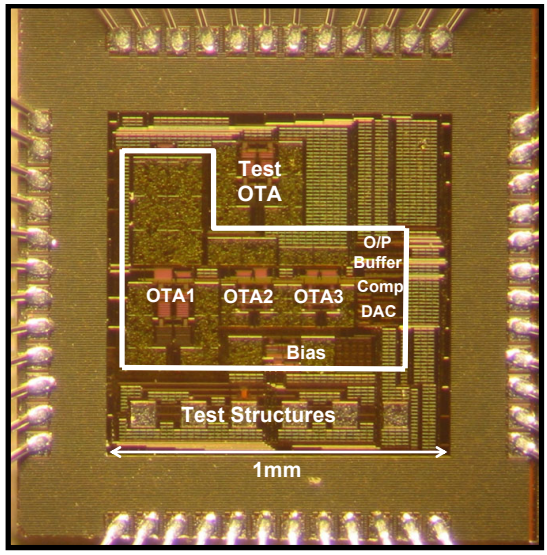

Figure 3.6.7: Die micrograph.

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